Amendments to the Claims:

1. (Withdrawn) A method of forming a wire bond structure in an integrated circuit (I/C) chip comprising the steps of:

providing an I/C chip having a conductive bond pad for attaching to a wire bond with at least one layer of dielectric material overlying the pad for the wire bond;

forming a surface defining an opening through said at least one layer of dielectric material to expose a portion of said bond pad for said wire bond;

forming at least a first conductive layer on said exposed surface of said bond pad for said wire bond and on the surface of said opening in said layer of dielectric material;

forming a seed layer on said first conductive layer;

applying a photoresist material over said seed layer;

exposing and developing said photoresist layer to reveal the surface of said seed layer surrounding said opening in said dielectric material;

removing the exposed upper seed layer;

removing the remaining photoresist material to reveal the remaining seed layer thereunder;

plating at least one second layer of conductive material on said remaining seed layer; and

removing the remaining portion of said first conductive layer on said dielectric layer around said opening.

2. (Withdrawn) The invention as defined in claim 1 wherein there are two layers of conductive material plated on said bond pad in said opening.

3. (Withdrawn) The invention as defined in claim 2 wherein said two layers of conductive material are Ni and Au.

4. (Withdrawn) The invention as defined in claim 1 wherein a seed layer underlies said at least one conductive layer overlying said bond pad.

5. (Withdrawn) The invention as defined in claim 4 wherein an intermediate conductive layer is provided between said seed layer and said bond pad.

6. (Withdrawn) The invention as defined in claim 5 wherein the intermediate conductive layer is TaN/Ta.

7. (Withdrawn) The invention as defined in claim 1 wherein the conductive pad in the I/C chip is Al.

8. (Withdrawn) The invention as defined in claim 1 wherein the dielectric layer is organic.

9. (Withdrawn) The invention as defined in claim 8 wherein a carbonaceous layer is formed on the dielectric layer underlying the TaN/Ta layer.

10. (Withdrawn) The invention as defined in claim 8 wherein the dielectric layer is photosensitive, and the opening therein is formed by photolithographic techniques.

11. (Currently amended) An I/C chip suitable for wire bonding comprising:

at least one conductive bond pad;

at least one layer of dielectric material overlying said conductive bond pad;

a surface defining an opening in said layer of dielectric material exposing said conductive bond pad; ~~and~~

a conductive seed layer disposed in said opening ~~at least one layer of conductive material~~ overlying said conductive bond pad and in contact therewith and in contact with the entire surface of said opening and having at least one exposed edge; and ~~also overlying and in contact with the entire surface of said opening~~

at least one layer of said conductive material overlying said conductive seed layer and completely covering said conductive seed layer including all exposed edges.

12. (Currently amended) The ~~invention~~ I/C chip as defined in claim 11 wherein there are two layers of conductive material plated on said conductive seed layer ~~bond pad~~ in said opening.

13. (Currently amended) The ~~invention~~ I/C chip as defined in claim 12 wherein said two layers of conductive material are Ni and Au.

14. (Canceled)

15. (Currently amended) The ~~invention~~ I/C chip as defined in claim 14 wherein an intermediate conductive layer is provided between said conductive seed layer and said conductive bond pad.

16. (Currently amended) The ~~invention~~ I/C chip as defined in claim 15 wherein the intermediate conductive layer is TaN/Ta.

17. (Currently amended) The ~~invention~~ I/C chip as defined in claim 11 wherein the conductive bond pad in the I/C chip is Al.

18. (New) The I/C chip as defined in claim 11 wherein said at least one layer of conductive material defines a wall in said I/C chip in which is disposed a ball bond and wire.

19. (New) The I/C chip as defined in claim 18 wherein the ball bond is Au.